Implementation of the communication chain for education

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***Abstract* - The aim of this article is to show a realization of the communication chain using a digital modulation. The whole communication chain concludes knowledge gained during the studies at our department of electrical engineering. It is mainly an application of programming, embedded systems programming, a digital modulation / a demodulation as a part of a digital signal processing, network communications and others. The paper is primarily focused on the application a modulator and a demodulator implemented into a FPGA (Field Programmable Gate Array) chip. The identification of synchronization sequence using NXOR (not exclusive logical disjunction) instead of Cross Correlation Function is introduced. Data transfer of three-dimensional data matrix is realized and Bit Error Rate is presented.**

Keywords - QPSK; FPGA; SoC; modulation; Ethernet; communication chain;

I. INTRODUCTION

Many papers have been written about signal modulation and demodulation. Most of them were focused on the theory of data transfer either from the modulation point of view or demodulation side. Another aspect of the data transfer is not commonly discussed and it is the pure realization of the communication data chain. For instance, the realization of the communication data chain can be used as teaching material in our faculty since it can be used in other scientific areas. The description of our communication chain is shown in Fig. 1 and although it is widely known, it still brings a few interesting issues which need to be solved.

The source data are generated using a program in a Personal Computer (PC) and these are transmitted via the Ethernet into the development kit SoCKit – current state-of-the-art chip Altera Cyclone V System on Chip (SoC). The modulator is realized into FPGA (Field Programmable Gate Array). Quadrature Phase Shift Keying was used as the modulation which is transferred. The first reason why the modulation was chosen is the linear state of the discreet part of a modulator. The second thing is to show something rarely understandable for students.

The modulated signal is converted from a digital time sequence to an analog form, and it is transferred via a kit (ME1000 RF) to a receiver part with the similar kit. There is a signal converted to intermediate frequency and converted to digital signal and transferred into the PC where is evaluated using the Key Performance Indicator (KPI) tests.

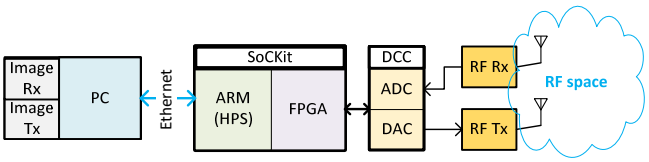

Figure 1. Block diagram of communication chain

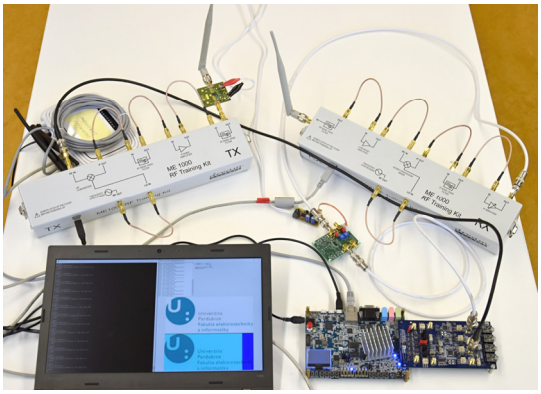

Figure 2. Components used to form the communication chain

This paper it mostly focused on a digital modulation and signal processing implementation into FPGA. Firmware of FPGA is written in a language VHDL (VHSIC Hardware Description Language) which was chosen as a widely used programming language. Most other parts of the chain are based on application programming and are described in various literatures [1], [2], [3].

The used communication pipeline is show in Fig. 2. The SoCKit and Data Convert Card are shown in a bottom together with PC. The upper part of the figure belongs to RF (Radio Frequency) kits.

II. HADRWARE

A. SoCKit

As the target platform Cyclone V SoC is was chosen. The target platform uses advantage of the SoC chip which contains FPGA chip Cyclone V and ARM (Acorn RISC Machine) processor Cortex A9 Dual-Core (the ARM part is called HPS - Hard Processor System) build in one integrated circuit (IC).

The IC provides us the advantages both – FPGA and ARM core as a one chip. It is price positive with lots of interfaces e.g. Ethernet, USB, display and others [4].

B. Data Convert Card

The Data Covert Card (DCC), originally from Terasic, is used for conversion between analog and digital signal (and vice versa). The DCC contains two 14-bits Analog to Digital converters (ADC) with sample rate 150 MSpS per channel as well as two 14-bit Digital to Analog converter (DAC) with sample rate 250 MSpS per channel. Others input/outputs are: Audio Codec with Line-In, Line-Out, MIC and Headphone output. The DCC is interconnected with the SoCKit via a High-Speed Mezzanine Card (HSMC) connector [5].

C. ME1000 RF

The ME1000 serves as a ready-to-teach package on RF circuits design in the areas of RF and Wireless communications. The RF transceiver kit consists of a transmitter and a receiver unit. The units are compounded from various RF modules to form both the transmitter and receiver sections of a super heterodyne system. The transceiver kit is controlled by Windows Control Panel software via USB. The block diagram is show in Fig. 3 [6]. Declared transmitting power is −4.5 dBm. The transmitter power amplifier ADL5605 was added between Tx kit and an antenna due to lack of power on reviver's site [7]. IF (Intermediate Frequency) of signal is supposed to be at frequency 50 MHz which is a requirement from the RF kit. RF transfer of the signal is realized at the carrier frequency 868 MHz.

III. IMPLEMENTAION

A. Quadrature Phase Shift Keying

Quadrature Phase Shift Keying (QPSK) modulation was chosen for demonstration of a communication chain implementation. QPSK is defined as:

$$s(t,\varphi) = A(t)\cos\left(2\pi f_{if} t + \varphi_i\right), \quad (1)$$

where φ_i has four different states (e.g. *+45°, +135°, -135°, -45°*) in digital phase modulation (2), phase is defined as (3).

$$s(t,m) = A\cos\left(2\pi f_{if} t + \theta_m\right), \quad (2)$$

$$\theta_m = 2\pi\frac{m-1}{M}, \quad (3)$$

where M is four (for QPSK modulation) and $m = 1, 2, \ldots, M$, is the modulation state [8]. Phase is supposed to be a constant during the symbol interval (T_s). The position of the points (binary coding – data symbol) represents the state of the modulator. The states are shown on Fig. 4.

B. Implemetaion QPSK modulation on FPGA

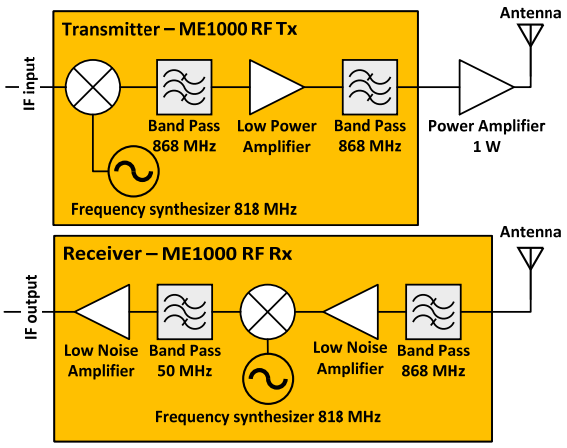

Figure 3. The block diagram of the transceiver kit (ME1000 RF)

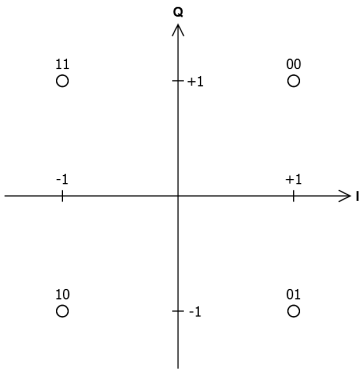

Figure 4. Used constellation diagram

TABLE 1. IQ STATE

Mod. state *m*	Data symbol	IQ State	
		I	*Q*
1	00	+	+
2	01	-	+
3	10	-	-
4	11	+	-

QPSK modulation is made using a quadrature modulator (4).

$$s(t - kT_s) = I(t - kT_s)\cos\left(2\pi f_{if} t\right) + Q(t - kT_s)sin(2\pi f_{if} t), \quad (4)$$

where I and Q are variables which indicate current state of the modulator, k is a number of data symbol. All four possible states modulator are summarized in Table 1.

The block diagram of the modulator is shown in Fig. 5 (data signals are represented by a black line, green lines are controls signals and clock signals are visualized by a blue line). Numbers at joints represent the signal bus width. Intellectual Property (IP) component NCO (Numerically Controlled Oscillator) generates harmonic signals for IQ (*I* – cos. signal,

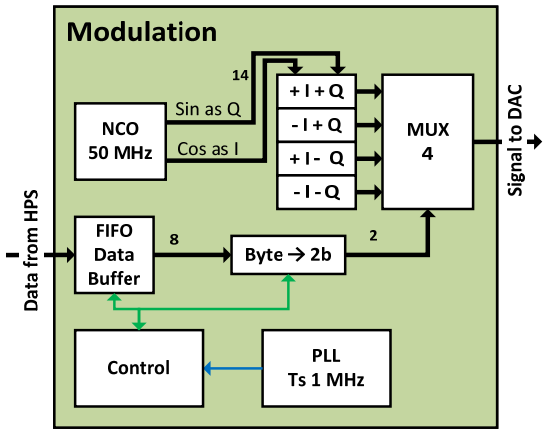

Figure 5. The block diagram of the modulation

Q – sin. signal) components at frequency 50 MHz [9], [10]. Desired status of the modulator is chosen based on input data and it stands for the whole time of modulation symbol T_s. Proposed solution does not guarantee a continuous phase between two consecutive symbols. Each symbol interval is generated using Phase-Lock Loop (PLL) at frequency 1 MHz for 1 ms. The output signal is propagated via 14-bit width bus which goes directly into DAC. Each transmission interval starts with a synchronization sequence. The main purpose of the sequence is the demodulator synchronization. The modulator block is derived by clock at 150 MHz (the same clock rate as DAC).

C. *Implemetaion QPSK demodulation on FPGA*

Demodulation uses a common conception of quadrature demodulator, where the outcomes of the block are I and Q components. The block diagram of the demodulation is in Fig. 6. The IF signal is sampled by ADC (125 MSpS) and filtered by a Band Pass (BP) FIR (Finite Impulse Response) filter. Bandwidth of the filter (at 3 dB drop against maxima) is 10 MHz, from 45 MHz up to 55 MHz. The stop band has attenuation -50 dB against minimum attenuation (63 fixed point coefficients). The results signal of 32-bit width is divided by bitwise to 14-bit width. As the base band signal is required the IF signal is mixed with the signals from the local oscillator derived from the NCO at the frequency 50 MHz. After mixing, filtering follows using a Low Pass Filter (LPF). The LPF has 5 MHz pass band and stop band has attenuation -50 dB from 10 MHz (25 fixed point coefficients). The filtered signal in base band is again divided by the bitwise to 17-bit length. For filtering, IP components of FIR II are used. The block of the demodulator is driven by clock at 125 MHz.

A standard procedure of the demodulation obtains phase (5) and amplitude (6) for each symbol interval. Nevertheless, VHDL is not that simply feasible realized the function *tan* and *root*. Therefore, data are obtained in different way than is usual.

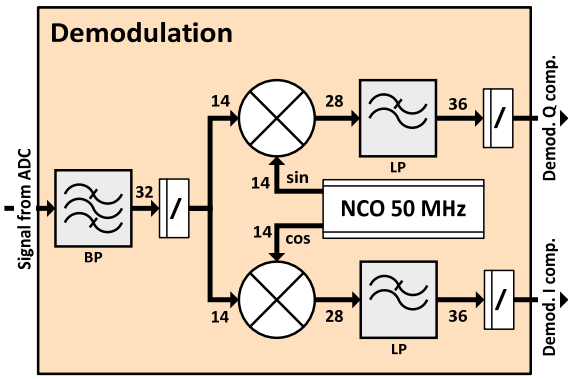

Figure 6. The block diagram of the demodulation

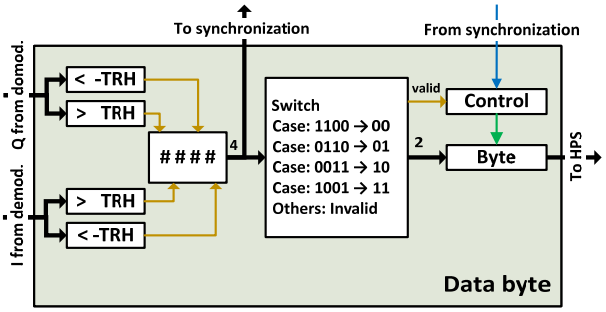

Figure 7. Signal processing of IQ component to data byte

$$\varphi = \tan^{-1}\frac{Q}{I} \tag{5}$$

$$a = \sqrt{I^2 + Q^2} \tag{6}$$

After demodulation, block data processing follows (Fig. 7). Course of I component is connected to two comparators (similarly the Q component).

One of the comparators has set limit positively and the second one negatively (6000 and -6000), signal has a width of 17-bit. These limits serve as indicators in the constellation diagram, see Fig. 8. Limits define areas which values of IQ components have to reach to be set as a valid. For instance, when the value of I component is greater than the positive threshold and the Q component is greater than the negative threshold, then the value of IQ represents a data symbol "11". The possible combinations are given in Table 2. For four status QPSK modulation are valid ones. Others are set as invalid. The bit is set if the value of the IQ component greater than the threshold. The bits are ordered [Q positive; I positive; Q negative; I negative], as 4-bit width signal.

The sequence of values from the comparators is used as input of the synchronization (sync) block (Fig. 9). The sync block is driven by clock at frequency 25 MHz and it is used as storage the signal of comparators. The memory has FIFO type (First In First Out) access. The memory depth is 100 samples of 4-bit width, which provides 25 samples for each T_s. The sync sequence is defined by Table 3.

TABLE 2. DEMODULATE DATA SYMBOL

Value from the comparators		Data symbol in T_s
Binary	*Decimal*	
1100	12	00
0110	6	01
0011	3	10
1001	9	11
Other combinations		*Invalid data symbol*

TABLE 3. SYNCHRONIZATION SEQUENCE

Correct comparators output for synchronization sequence						
value	1100	1100	1100	0110	0110	0110
sample	0	…	24	25	…	49
value	0011	0011	0011	1001	1001	1001
sample	50	…	74	75	…	99

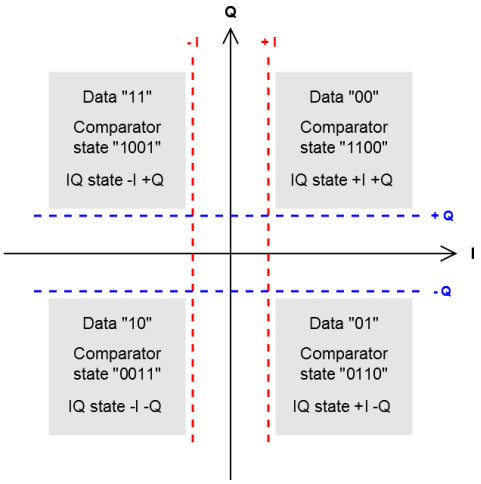

Figure 8. The constellation diagram with possible comparators states

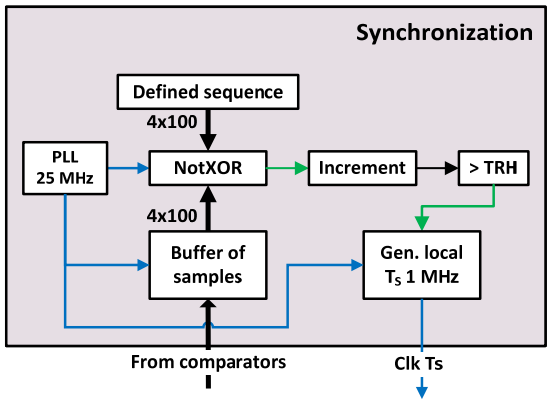

Figure 9. The block scheme of the synchronization

As comparison between input data and the reference data is needed, the same memory (type and width) is used as storage for reference data. In many cases, where the comparison between two signals is needed the correlation is used [8]. The same principle is used in our case as well. A correlation function uses multiplication which is computationally expensive; therefore NXOR (not exclusive logical disjunction) is used to speed up an identification of the synchronization sequence. If the NXOR function returns the value "1111" the received sample has match with synch sequence, moreover the counter is incremented by one. If the counter is higher than certain threshold, which is empirically set to 80, the local clock T_s is synchronized.

D. Comunication betwen PC and SoCKit

Communication between PC and SoCKit is socket based communication (using Ethernet with TCP-IP protocol). The program routine in the ARM initializes a socket server. The program routine in the PC runs as a socket client and connects to the server. Program in ARM sends the received data to FPGA (to FIFO buffer in the modulator). Conversely, data received from of the demodulator are collected in the packet (one column of image), and sent to the PC, where the original image assembled.

IV. Results

A dataset is a picture and it is expressed as a 3D matrix of size *75* x *150* x *3* (*Height* x *Width* x *Color*) pixels. The program (client) gradually sends the selected column from the data array, with the same color, to the server. The client counts a number of correctly received pixels as well as number of pixels which were received incorrectly, see Table 4.

TABLE 4. TYPICAL TRANSFER VALUES

Baud Rate [B/s]	Wrong Bytes	BER	Wrong Pixels	KPI	Wrong packet
200	625	0.0159	96	0.73	0
1000	712	0.0181	113	0.86	0
5000	6148	0.1561	309	2.35	17

V. Conclusion

The output signal from the RF receiver is very low and close to noise floor (the order of -50 dBm) and it has to be amplified in order for the full dynamics of ADC scale to be utilized. Neither packets communication nor secure transmission is used, for simplicity reason. This has the effect that some of the data are not transmitted correctly. Error in socket communication manifests faulty pixels in the image columns (in the socket carries the entire column one color component). Data transfer rate of the communication chain is decelerated to maximally 5000 B/s, otherwise BER is higher than 0.16 (ca. 6000 wrong bytes of 39375 B) and average number of wrong pixels is ca. 150 (KPI is 1.3%). Transfer of the whole picture takes approximately 40 seconds with Baud Rate 1000 B/s.

A designed communication chain was introduced and it will be used in educational subjects: such as programming, signal processing, modulation/demodulation theory and

practice and many more, as well as an idea to identify synchronization sequence using NXOR at the receiving site.

In the future, the signal processing will be included in: packet format data transmission and repaired or upgraded minor problems that arose during implementation. To reduce the error, it would be appropriate to apply a constellation diagram derived from Gray coding and add a check sum.

ACKNOWLEDGMENT

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