Comparison of Positive and Negative Dickson Charge Pump and Fibonacci Charge Pump

David Matoušek Department of Electrical Engineering University of Pardubice 530 02 Pardubice, Czech Republic david.matousek@upce.cz

Abstract - An operation of electronic equipment is dependent on a power supply. Today, a trend of only one AC/DC adapter is used for supplying an electronic system. Thus, an electronic equipment with various power supply requirements uses some internal DC/DC converters. These DC/DC converters adjust input voltage to lower or/and higher value or generate a negative voltage. The classical DC/DC converters are based on inductors or transformers. These converters are too large and suitable for a higher output power. A charge pumps are a sufficient alternative to classical DC/DC converters for a lower output power and a smaller dimension. A well-known variant of a charge pump is Dickson charge pump. The output to input voltage ratio is a directly proportional to the number of Dickson charge pump stages. Thus, the number of stages can be a relatively high for low input voltage and required high output voltage. The Fibonacci charge pump is a suitable alternative to Dickson charge pump especially for a higher output to input voltage ratio. This article describes practical circuit solution of the Fibonacci charge pump. The key properties of the Dickson and the Fibonacci pumps are compared in this article, too.

Keywords-Dickson charge pump; Fibonacci charge pump; negative charge pump; voltage gain.

I. CHARGE PUMP TOPOLOGY

Dickson charge pump [1], [2], [3] topology for positive output voltage is shown in Fig. 1. The boxes marked 1 or 2 represent switches. The switch is in ON state for the odd phase (1) or the even phase (2).



Figure 1. The topology of positive Dickson charge pump.

The voltages in nodes V_1 to V_4 are gradually increased about a constant voltage gain ΔV . Ideally, the voltage gain has the same value as input voltage V_{IN} , thus $\Delta V = V_{IN}$. The ideal no-load output voltage V_{OUT} of positive Dickson charge pump of the Nth order applies accorded to [1] (1). Ladislav Beran Department of Electrical Engineering University of Pardubice 530 02 Pardubice, Czech Republic

$$V_{OUT} = V_{IN} \cdot (N+1) \tag{1}$$

where V_{IN} and V_{OUT} are the input and output voltages, N is the number of stages.

Dickson charge pump topology for negative output [4] voltage is shown in Fig. 2.



Figure 2. Topology of negative Dickson charge pump.

The voltages in nodes V_1 to V_4 are gradually decreased about a constant voltage gain ΔV . Ideally, $\Delta V = -V_{IN}$. The ideal no-load output voltage V_{OUT} of negative Dickson charge pump of the Nth order applies according (2).

$$V_{OUT} = -V_{IN} \cdot N \tag{2}$$

where V_{IN} and V_{OUT} are the input and output voltages, N is the number of stages.

Fibonacci charge pump [5], [6] topology for positive output voltage is shown on Fig. 3.



Figure 3. The topology of positive Fibonacci charge pump.

The voltages in nodes V_1 to V_4 are gradually increased about a variable voltage gain ΔV_n . The value of the voltage gain ΔV_n accords to Fibonacci numbers (1, 1, 2, 3, 5, 8, ...). Ideally, values of the voltage gain for Fibonacci charge pump of the 4th order are: $\Delta V_1 = V_{IN}$, $\Delta V_2 = V_{IN}$, $\Delta V_3 = 2 \cdot V_{IN}$, $\Delta V_4 = 3 \cdot V_{IN}$. The sum of the voltage gains ΔV_n is the same as the sum of the Fibonacci numbers (3).

The published research results were supported by the Internal Grant Agency of University of Pardubice, the project SGS 2017 030.

$$SF(N) = \sum_{n=1}^{N} F_n \tag{3}$$

where SF(N) is a sum of the Fibonacci numbers to the *N*th order, F_n is the Fibonacci number of the *n*th order.

The ideal no-load output voltage V_{OUT} of the positive Fibonacci charge pump of the Nth order applies according (4). For example, for N = 4 the ideal no-load output voltage is $V_{OUT} = 8 \cdot V_{IN}$.

$$V_{OUT} = V_{IN} \cdot \left[SF(N) + 1 \right] \tag{4}$$

where V_{IN} and V_{OUT} are the input and output voltages, SF(N) refers to (3).

Fibonacci charge pump topology for negative output voltage is derived from Fig. 3 and shown on Fig. 4.



Figure 4. Topology of negative Fibonacci charge pump.

The voltages in nodes V_1 to V_4 are gradually decreased about a variable voltage gain ΔV_n . The ideal no-load output voltage V_{OUT} of the negative Fibonacci charge pump of the Nth order applies according (5).

$$V_{OUT} = -V_{IN} \cdot SF(N) \tag{5}$$

where V_{IN} and V_{OUT} are input and output voltages, SF(N) refers to (3).

II. CHARGE PUMPS REALISATION

Presented charge pumps are used for supplying analogue part of a complex electronic system from 3 V DC adapter. This analogue part uses dual power supply -18 V approx. and +21 V approx. with current consumption 1.5 mA.

A charge pump usage is fully sufficient for solving this problem. A negative charge pump generates the output voltage six times higher than the input voltage. A positive charge pump generates the output voltage seven times higher than the input voltage. But these calculations are valid for no-load output and the ideal value of the voltage gain only. Practically, the number of stages of proposed charge pumps must be increased about one minimally. Thus, the negative and positive Dickson charge pump have seven stages. Similarly, the negative and positive Fibonacci charge pump have four stages. The no-load output voltages are -21 V and +24 V ideally for the both variant of charge pumps. The key parameters of proposed charge pumps were verified by simulation in LTspice XVII.

The key problem of a practical charge pump realization is an implementation of switches. Especially, a floating switch realization and its driving are very complicated.

Dickson charge pumps use the floating switches connected between input and output of each stage (see Fig. 1 or Fig. 2). These switches can be realised by diodes. The diode switches automatically, thus we don't have to solve the problem of generating driving signal for this switch. The Schottky diode is used for a low value of the diode forward voltage drop.

A well-known variant of Dickson charge pump for positive or negative output voltage is shown in Fig. 5 [1] or Fig. 6 [2] respectively. Transistors M_1 , M_2 and M_3 , M_4 realize inverters for generating odd and even phase of clocking signal.



Figure 5. Practical realization of positive Dickson charge pump of the 7th order.



Figure 6. Practical realization of negative Dickson charge pump of the 7th order.

Fibonacci charge pumps use two floating switches (see Fig. 3 and Fig. 4). We designed circuits by Fig. 7 and Fig. 8 that inspired [7]. The switch between input and output of each stage can be realized by Schottky diode similarly to Dickson charge pump. Transistors M_{xa} , M_{xb} (where x indicates the number of the stage) drive capacitor C_x , and transistors M_{xc} , M_{xd} are used for driving a next stage (x+1).



Figure 7. Practical realization of positive Fibonacci charge pump of the 4th order.



Figure 8. Practical realization of negative Fibonacci charge pump of the 4th order.

We assume realization of these charge pumps in discrete form. Firstly, we select the transistors in relation to the input voltage; the threshold voltage of used transistors is about ± 2 V. Secondly, we select Schottky diode in relation to a low value forward voltage drop (used variant has $V_F = 150$ mV only). Finally, we calculate the capacitance of the transfer and load capacitor from (6). The consumed current is $I_{OUT} = 1.5$ mA and the absolute value of the output voltage V_{OUT} is 18 V or 21 V. We assume the rise time of the output $t_R = 25$ ms. We calculate values of the capacitance 2.1 μ F and 1.8 μ F. The load and transfer capacitance was set to value $C_{LOAD} = C_T = 2.2 \ \mu$ F.

$$C_{LOAD} = \frac{I_{OUT} \cdot t_R}{V_{OUT}} \tag{6}$$

where C_{LOAD} is the capacitance of the transfer capacitor, I_{OUT} is the consumed current, t_R is the rise time of the output voltage, V_{OUT} is the output voltage.

The parameters of used devices are clearly listed in Table I.

TABLE I. PARAMETERS OF USED DEVICES

Device	Туре
NMOS transistor	2N7002
PMOS transistor	BSS84
Schottky diode	PMEG4010BEA
Transfer and load capacitor	2.2 μF/50 V
Clocking frequency	33 kHz

III. RESULTS FROM SIMULATIONS

Proposed realization of presented charge pumps (CP) was verified by simulations in LTspice XVII. The key parameters were the output voltage, efficiency (7), rise time and ripple voltage of the output.

$$\zeta = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot I_{IN}} \cdot 100\%$$
⁽⁷⁾

where ζ is efficiency, V_{OUT} , I_{OUT} are output voltage and current, V_{IN} , I_{IN} are input voltage and current.

The positive variant of Dickson charge pump (DCP) and Fibonacci charge pump (FCP) are compared firstly.



Figure 9. Graph of the output voltage as a function of the output current (load characteristic) for positive charge pumps.

FCP has a lower series resistance, thus FCP is usable for higher values of the output current (see Fig. 9). Similarly, the efficiency of FCP is higher than the efficiency of DCP for output currents higher than approx. 3 mA (see Fig. 10). Other parameters are listed in Table II.



Figure 10. Graph of the efficiency as a function of the output current for positive charge pumps.

TABLE II. SIMULATED PARAMETERS OF POSITIVE CPS

Parameter	DCP	FCP
Output voltage V _{OUT}	21.45 V	20.80 V
Efficiency ζ	88.6 %	77.9 %
Ramp-up time t _R	22.7 ms	7.4 ms
Ripple voltage p-p V _R	10 mV	10 mV
Number of stages N	7	4

The negative variant of FCP has a higher efficiency than DCP over the full observed range. The negative FCP has a lower series resistance than DCP, thus the rise time of FCP is a lower than for DCP.



Figure 11. Graph of the output voltage as a function of the output current (load characteristic) for negative charge pumps.



Figure 12. Graph of the efficiency as a function of the output current for negative charge pumps.

TABLE III. SIMULATED PARAMETERS OF NEGATIVE CPS

Parameter	DCP	FCP
Output voltage V _{OUT}	-18.45 V	-17.87 V
Efficiency ζ	73.8 %	75 %
Ramp up time t _R	24.2 ms	6.4 ms
Ripple voltage p-p V _R	11 mV	11 mV
Number of stages N	7	4

IV. CONCLUSION

The principle of Dickson charge pump and Fibonacci charge pump for generating positive and negative voltage was presented.

Presented practical realization of these charge pumps were verified by simulation in LTspice XVII with discrete transistors, diodes and capacitors.

The Fibonacci charge pumps use a lower number of stages, and have a lower internal series resistance and a lower rise time. These charge pumps are suitable for a higher output current, especially. Dickson charge pumps have a primitive structure but use a higher number of capacitors. The proposed Dickson charge pumps use 16 capacitors, but Fibonacci charge pumps use 10 capacitors only.

REFERENCES

- J. F. Dickson, On-Chip high-voltage generation in NMOS integrated circuits using an improved voltage multiplier technique", IEEE Journal of Solid-State Circuits, vol. 11, no. 3, pp. 374-378, 1976.
- [2] F. Pan, T. Samaddar, Charge Pump Circuit Design, McGraw-Hill, New York, 2006.
- [3] G. Palumbo, D. Pappalardo, "Charge pump circuits: An overview on design strategies and topologies", IEEE Circuits and Systems Magazine, First Quarter 2010, 1531-636X/10, IEEE 2010, pp. 31-45.
- [4] T. Yamazoe, H. Ishida, Y. Nihongi, "A charge pump that generates positive and negative high voltages with low power-supply voltage and low power consumption for nonvolatile memories", In: International Symposium ISCAS, Taipei, Taiwan, 2009, pp. 988-991.
- [5] F. Ueno, T. Inoue, I. Oota, I. Harada. "Emergency power supply for small computer systems". In proceedings of IEEE International Conference Circuits and System, pp. 1065-1068, 1991.
- [6] T. Tanzawa. "Innovation of Switched-Capacitor Voltage Multiplier, Part 1: A brief history". IEEE Solid-State Circuits Magazine, pp. 51-59, 2016.
- [7] D. Matousek, O. Subrt, J. Hospodka, "Charge pump design for use in NVM device test and measurement", In: MEASUREMENT 2015, Proceedings of the 10th International Conference, Smolenice, 2015, pp. 203-206.